REMARKS

Reconsideration and allowance are respectfully requested in light of the above amendments and the following remarks.

Claims 15-20 have been canceled. Independent claims 21 and 25 have been amended and claims 29 and 30 newly added to better define the subject matter that the Applicants regard as the invention. Support for the revisions of claims 21 and 25 is provided in the specification on page 12, last paragraph, and page 16, second paragraph. Support for the subject matter of claims 29 and 30 is provided in the specification on page 13, last paragraph.

Claims 21-24 and 27 were rejected, under 35 USC §103(a), as being unpatentable over Inata et al. (US 4,593,301) in view of Nakamura (JP 03250742). Claims 25, 26, and 28 were rejected, under 35 USC §103(a), as being unpatentable over Inata in view of Shakuda (US 5,825,052). To the extent these rejections may be deemed applicable to the revised claims, the Applicants respectfully traverse.

With the conventional method of activating the ion implanted regions of an FET, Si donors in the carrier supply layer or active layer and the F atoms on the substrate surface form compound matter by the high temperature annealing process, at the time of forming the source/drain area. As a result, the carrier

density is reduced, and the FET characteristics are degraded. In view of the above, the claimed invention uses Se donors or Te donors in the carrier supply layer. Se and Te require a high amount of energy to bind with the F atom. As a result, the Se donors or Te donors do not form compound matter easily with the F atoms, unlike the case of Si donors. Therefore, these atoms are used as doping impurities. Thus, even if the high temperature annealing process is performed, it is possible to produce a heterojunction FET without significantly degrading the FET characteristics.

In view of the sheet carrier density (the effect is large when the temperature is higher than 450°C) in Fig. 4 and degradation or activation at the heterojunction interface, it is preferable that the annealing temperature is in the range of 700°C to 850°C.

None of the references discloses or suggests that the F atoms are present on the substrate surface and cause the adverse affect. In Inata, Nakamura and Shikuda, although there are statements regarding the annealing temperature, the optimum temperature recited in new claims 29 and 30 is not obvious based on those statements.

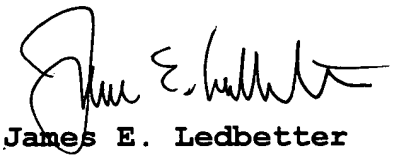
Accordingly, the Applicants respectfully submit that the applied references do not teach or suggest the subject matter of

independent claims 21 and 25. Therefore, allowance of claims 21 and 25 and all claims dependent therefrom is warranted.

In view of the above, it is submitted that this application is in condition for allowance and a notice to that effect is respectfully solicited.

If any issues remain which may best be resolved through a telephone communication, the Examiner is requested to telephone the undersigned at the local Washington, D.C. telephone number listed below.

Respectfully submitted,



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